19-2934; Rev 0; 7/03

MAXIM

10Gbps Modulator Driver

General Description

The MAX3942 is designed to drive high-speed optical modulators at data rates up to 10.7Gbps. It functions as a modulation circuit, with an integrated control op amp externally programmed by a DC voltage.

A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. When a clock signal is available, the integrated data-retiming function can be selected to reject input-signal jitter.

The MAX3942 receives differential CML signals (ground-referenced) with on-chip line terminations of 50Ω. Each of the differential outputs has an on-chip 50Ω resistor for back termination. The driver is able to deliver a modulation current of 40mA$_{P-P}$ to 120mA$_{P-P}$, with an edge speed of 23ps (typical 20% to 80%). This modulation current reflects a modulation voltage of 1.0V$_{P-P}$ to 3.0V$_{P-P}$ single ended or 2.0V$_{P-P}$ to 6.0V$_{P-P}$ differential.

The MAX3942 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical modulator characteristics. It is available in a compact 4mm × 4mm, 24-pin thin QFN package and operates over the -40°C to +85°C temperature range.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3942ETG	-40°C to +85°C	24 Thin QFN (4mm × 4mm)

Features

- **23ps Edge Speed**
- **Single-Ended Modulation Voltage Up to 3V$_{P-P}$**
- **Differential Modulation Voltage Up to 6V$_{P-P}$**
- **Selectable Data-Retiming Latch**
- **Up to 10.7Gbps Operation**
- **50Ω On-Chip Input and Output Terminations**
- **Pulse-Width Adjustment**
- **Enable and Polarity Controls**
- **ESD Protection**

Applications

Mach Zehnder Modulators

Packaged Direct-Modulated Lasers

SONET OC-192 and SDH STM-64 Transmission Systems

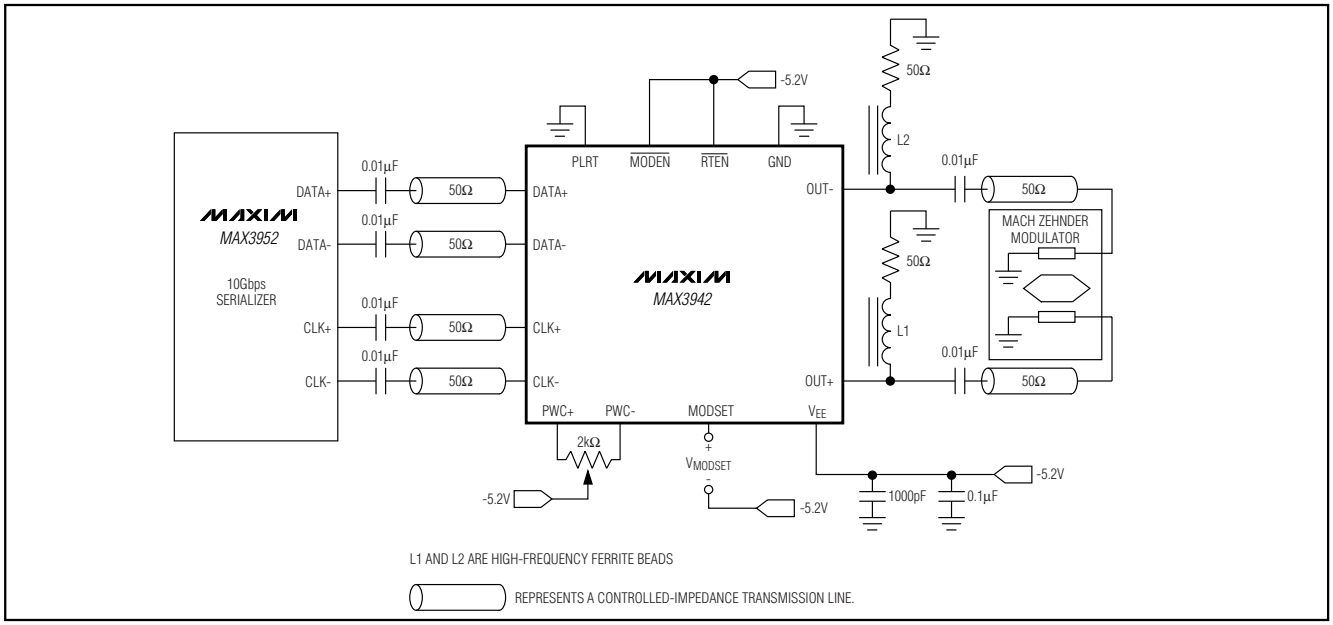
DWDM Systems

Long/Short-Reach Optical Transmitters

10Gbps Ethernet

Pin Configuration appears at end of data sheet.

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{EE} .....-6.0V to +0.5V
Voltage at $\overline{MODEN}$, $\overline{RTEN}$, PLRT, MODSET.....(V_{EE} - 0.5V) to +0.5V
Voltage at DATA+, DATA-, CLK+, and CLK-.....-1.65V to +0.5V
Voltage at OUT+, OUT- .....-4V to +0.5V
Voltage at PWC+, PWC- .....(V_{EE} - 0.5V) to (V_{EE} + 1.7V)
Continuous Power Dissipation (T_A = +85°C)
24-Pin Thin QFN (derate 20.8mW/° above +85°C) 1354mW
Current into or out of OUT+, OUT-.....80mA
Storage Temperature Range .....-55°C to +150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.5V to -4.9V, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, I_{MOD} = 100mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{EE}			-5.5		-4.9	V
Supply Current	I_{EE}	Excluding I_{MOD} (Note 1)	Retime disabled		125	175	mA
			Retime enabled		140	200	
Power-Supply Noise Rejection	PSNR	f ≤ 2MHz (Note 2); see Figure 3			15		dB
SIGNAL INPUT (Note 3)							
Input Data Rates		NRZ			10.7		Gbps
Single-Ended Input Resistance	R_{IN}	Input to GND		42.5	50	58.5	Ω
Single-Ended Input Voltage	V_{IS}	DC-coupled, Figure 1a		-1		0	V
		AC-coupled, Figure 1b		-0.4		+0.4	
Differential Input Voltage	V_{ID}	DC-coupled (Note 4)		0.2		2.0	V_{P-P}
		AC-coupled (Note 4)		0.2		1.6	
Differential Input Return Loss	RL_{IN}	≤ 15GHz			15		dB
MODULATION (Note 5)							
Maximum Modulation Current				112	120		mA_{P-P}
Minimum Modulation Current		V_{MODSET} = V_{EE}			37	40	mA_{P-P}
MODSET Voltage Range	V_{MODSET}			V_{EE}		V_{EE} + 1	V
Equivalent Modulation Resistance	R_{MODEQV}	(Note 7)			11.1		Ω
Modulation Set Bandwidth		Modulation depth 10%, 50Ω driver load			5		MHz
MODSET Input Resistance					20		kΩ
Modulation-Current Temperature Stability		(Note 6)		-980		0	ppm/°C
Modulation-Current-Setting Error		50Ω driver load, T_A = +25°C		-10		+10	%
Output Resistance	R_{OUT}	OUT+ and OUT- to GND		42.5	50	58.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.5V to -4.9V, T_A = -40°C to +85°C. Typical values are at V_{EE} = -5.2V, I_{MOD} = 100mA, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Off Current		$\overline{MODEN}$ = V_{EE}, MODSET = V_{EE}, DATA+ = high, DATA- = low				1.6	mA
Differential Output Return Loss	RL_{OUT}	I_{MOD} = 50mA	≤ 10GHz		10		dB
Output Edge Speed		20% to 80% (Notes 6, 8)			23	32	ps
Setup/Hold Time	t_{SU}, t_{HD}	Figure 2 (Note 6)		25			ps
Pulse-Width Adjustment Range		(Notes 6, 8)		±30	±50		ps
Pulse-Width Control Input Range (Single Ended)		For PWC+ and PWC-		V_{EE} + 0.5		V_{EE} + 1.5	V
Pulse-Width Control Input Range (Differential)		(PWC+) - (PWC-)		-0.5		+0.5	V
Output Overshoot	δ	(Notes 6, 8)			5		%
Driver Random Jitter	RJ_{DR}	(Note 6)			0.3	0.8	ps_{RMS}
Driver Deterministic Jitter	DJ_{DR}	PWC- = GND (Notes 6, 9)			8	13	ps_{P-P}
CONTROL INPUTS							
Input High Voltage	V_{IH}	(Note 10)		V_{EE} + 2.0			V
Input Low Voltage	V_{IL}	(Note 10)				V_{EE} + 0.8	V
Input Current		(Note 10)		-80		+200	µA

Note 1: Supply current remains elevated once the retiming function has been enabled. Power must be cycled to reduce supply current after the retiming function has been disabled.

Note 2: Power-supply noise rejection is specified as PSNR = 20Log($V_{noise\ (on\ Vcc)}$ / ΔV_{OUT}). V_{OUT} is the voltage across a 50Ω load. $V_{noise\ (on\ Vcc)}$ = $100mV_{P-P}$.

Note 3: For DATA+, DATA-, CLK+, and CLK-.

Note 4: CLK input characterized at 10.7Gbps.

Note 5: Minimum voltage on OUT+ and OUT- is V_{EE} + 1.9V.

Note 6: Guaranteed by design and characterization using the circuit shown in Figure 3.

Note 7: R_{MODEQV} = (V_{MODSET} - V_{EE}) / (I_{MOD} - 37mA).

Note 8: 50Ω load, characterized at 10.7Gbps with a 1111 1111 0000 0000 pattern.

Note 9: Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Measured with a 10.7Gbps 2^7 - 1 PRBS pattern with 80 zeros and 80 ones inserted in the data pattern.

Note 10: For $\overline{MODEN}$ and PLRT.

10Gbps Modulator Driver

Test Circuits and Timing Diagrams

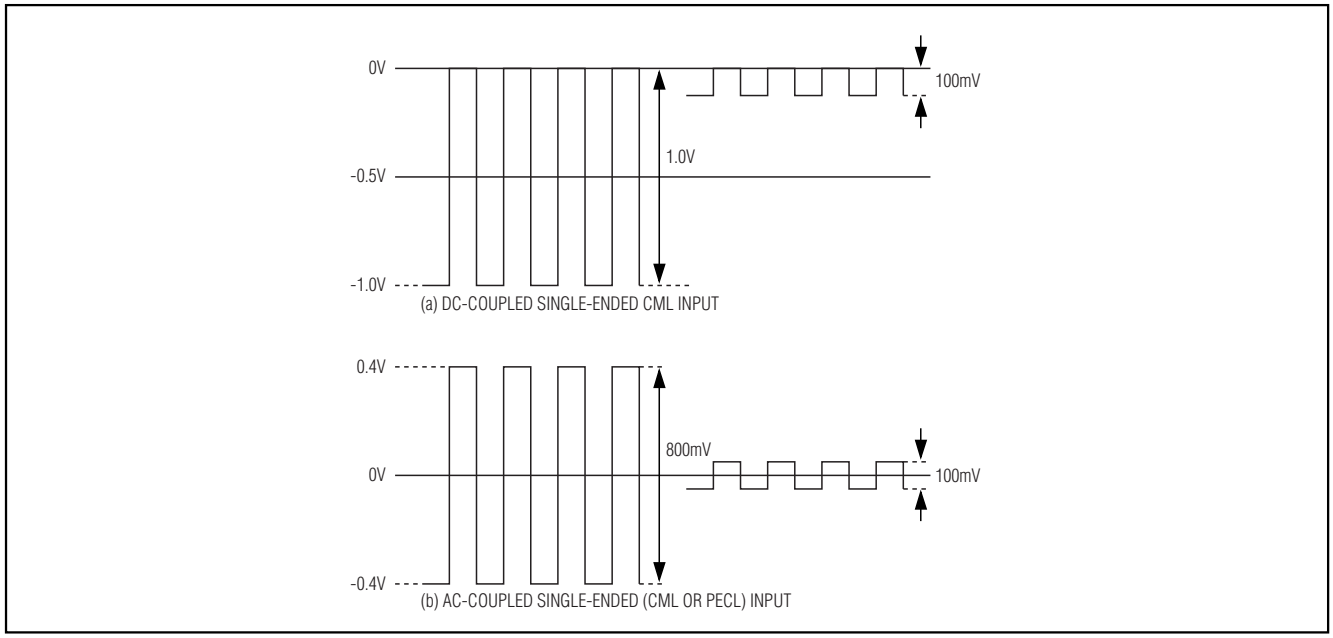


Figure 1. Definition of Single-Ended Input Voltage Range

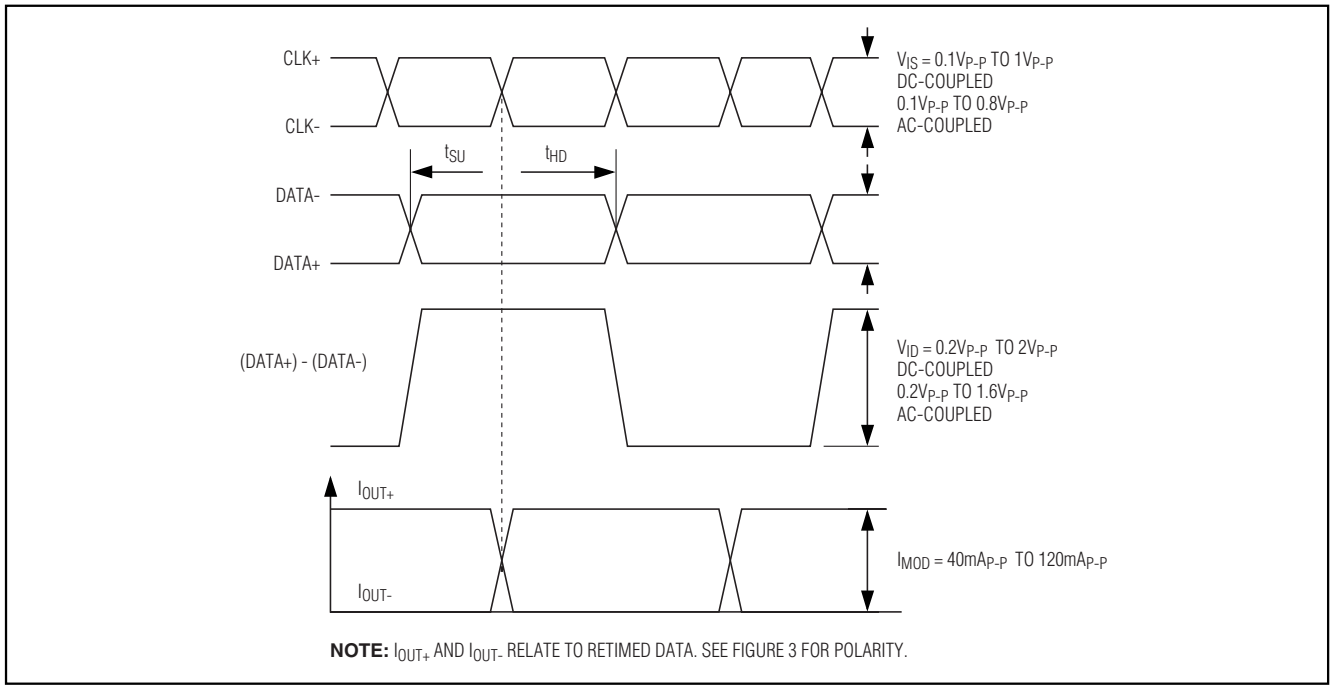


Figure 2. Setup and Hold Timing Definition

Test Circuits and Timing Diagrams (continued)

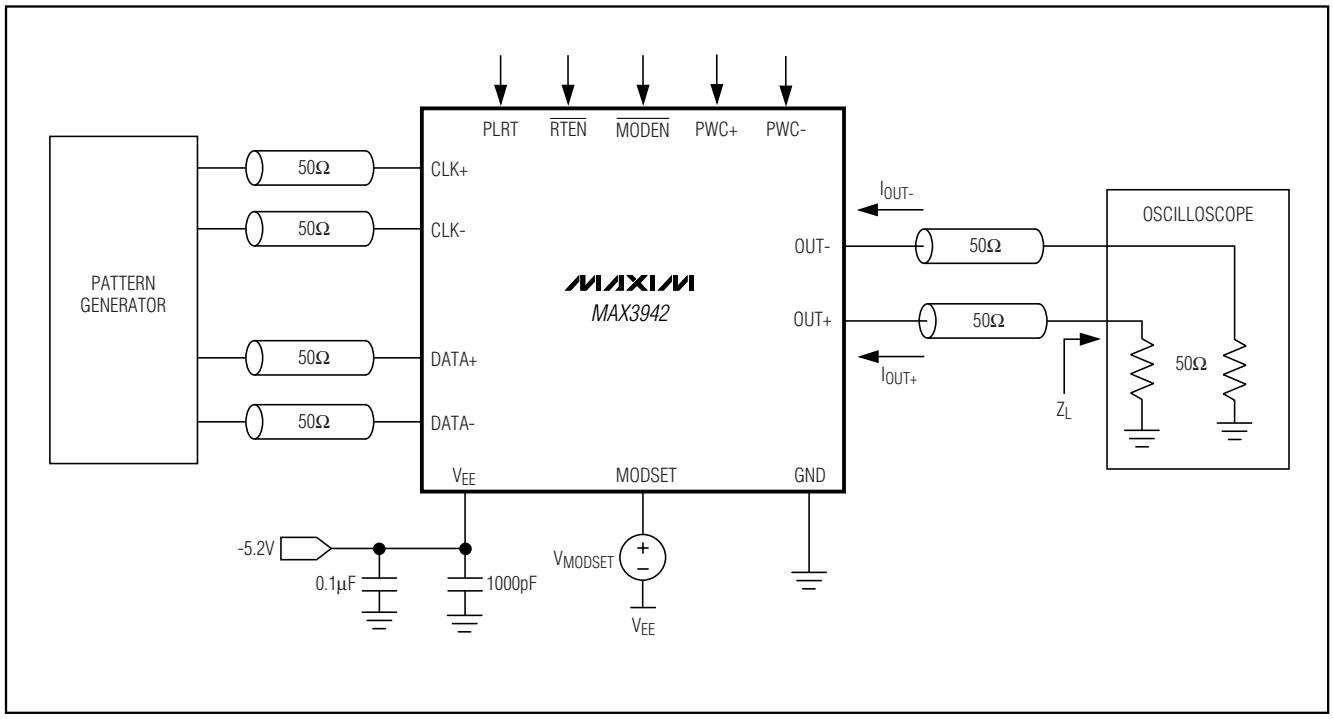


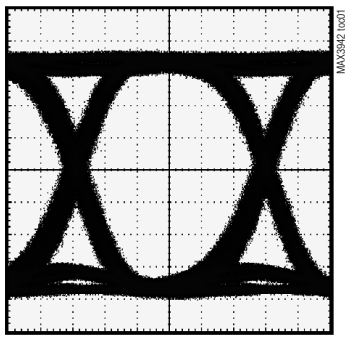
Figure 3. AC Characterization Circuit

10Gbps Modulator Driver

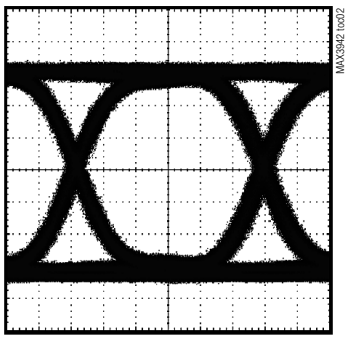
Typical Operating Characteristics

(Typical values are at V_{EE} = -5.2V, I_{MOD} = 100mA, T_A = +25°C, unless otherwise noted.)

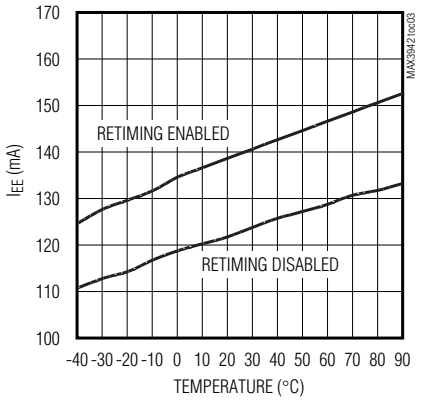
10.7Gbps ELECTRICAL EYE DIAGRAM (V_{MOD} = 2V_{P-P} DIFFERENTIAL, 2^{31} - 1 PRBS)



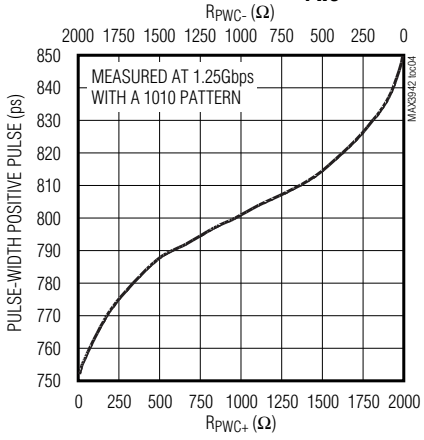
10.7Gbps ELECTRICAL EYE DIAGRAM (V_{MOD} = 6V_{P-P} DIFFERENTIAL, 2^{31} - 1 PRBS)



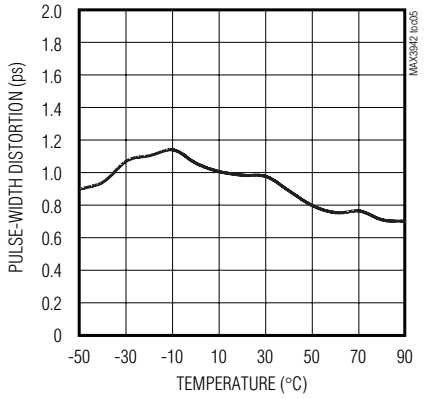
SUPPLY CURRENT vs. TEMPERATURE (50Ω LOAD, EXCLUDES I_{MOD})



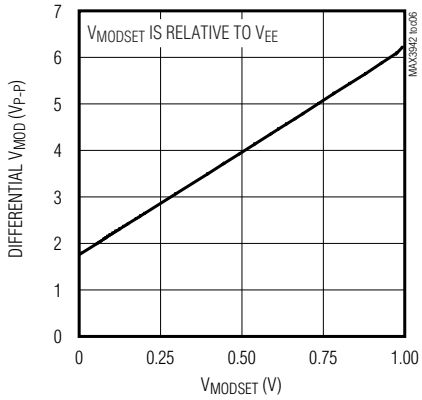
PULSE WIDTH vs. R_{PWC}



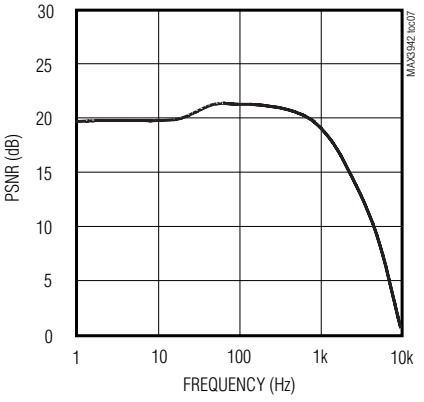
PULSE-WIDTH DISTORTION vs. TEMPERATURE



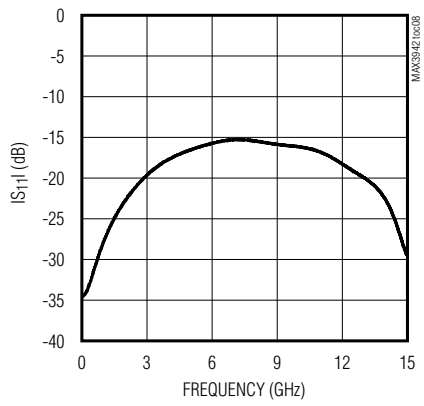
DIFFERENTIAL V_{MOD} vs. V_{MODSET} (Z_L = 50Ω ON OUT+ AND OUT-)



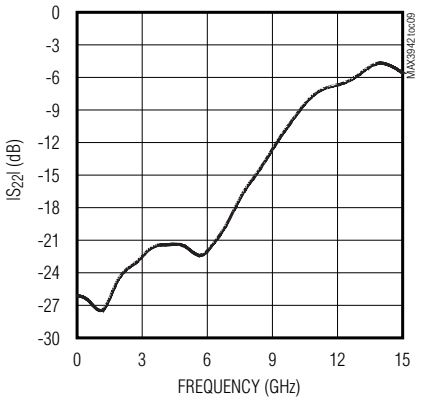
POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



DIFFERENTIAL S_{11} vs. FREQUENCY (DEVICE POWERED)



DIFFERENTIAL S_{22} vs. FREQUENCY (DEVICE POWERED)



Pin Description

PIN	NAME	FUNCTION
1	DATA+	Noninverting Data Input, with 50Ω On-Chip Termination
2	DATA-	Inverting Data Input, with 50Ω On-Chip Termination
3, 4, 14, 17	GND	Ground. All pins must be connected to board ground.
5	CLK+	Noninverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
6	CLK-	Inverting Clock Input for Data Retiming, with 50Ω On-Chip Termination
7, 11, 12, 13, 18, 19, 21, 24	V_{EE}	Negative Supply Voltage. All pins must be connected to board V_{EE}.
8	PWC+	Positive Input for Modulation Pulse-Width Adjustment (see the *Design Procedure* section).
9	PWC-	Negative Input for Modulation Pulse-Width Adjustment. Ground to disable the pulse-width adjustment feature (see the *Design Procedure* section).
10	MODSET	Modulation Current Set. Apply a voltage to set the modulation current of the driver output.
15	OUT-	Inverting Driver Output. Provides modulation output with 50Ω back termination. Sinks current when PLRT is high and when differential data is high.
16	OUT+	Noninverting Driver Output. Provides modulation output with 50Ω back termination. Sinks current when PLRT is high and when differential data is low.
20	PLRT	Differential Data Polarity Swap Input. Set high or float for normal operation. Set low to invert the differential signal polarity. Contains an internal 100kΩ pullup to GND.
22	$\overline{MODEN}$	TTL/CMOS Modulation Enable Input. Set low or float for normal operation. Set high to put the EAM in the absorption (logic 0) state. Contains an internal 100kΩ pulldown to V_{EE}.
23	$\overline{RTEN}$	Data-Retiming Input. Connect to V_{EE} for retimed data. Connect to GND to bypass retiming latch.
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance. See the *Layout Considerations* section.

Detailed Description

The MAX3942 modulator driver accepts differential clock and data inputs that are compatible with PECL and CML logic levels.

The modulation output stage is composed of a high-speed differential pair and a programmable current source with a maximum modulation current of 120mA. The rise and fall times are typically 23ps. The modulation current is designed to produce a modulation voltage up to $3.0V_{P-P}$ single endedly, or $6.0V_{P-P}$ differentially when driving a 50Ω module. The $3.0V_{P-P}$ results from $120mA_{P-P}$ through the parallel combination of the 50Ω modulator load and the internal 50Ω back termination.

Polarity Switch

The MAX3942 includes a polarity switch. When the PLRT pin is high or left floating, the outputs maintain the polarity of the input data. When the PLRT pin is low, the outputs are inverted relative to the input data.

Clock/Data Input Logic Levels

The MAX3942 is directly compatible with ground-reference CML. Either DC- or AC-coupling may be used for CML referenced to ground. For all other logic types, AC-coupling should be used.

Optional Data Input Latch

To reject pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{RTEN}$ control input should be connected to V_{EE}.

The input data is retimed on the rising edge of CLK+. If RTEN is connected to ground, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

Pulse-Width Control

The pulse-width control circuit can be used to compensate for pulse-width distortion introduced by the modulator. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. The adjustment range is typically ±50ps. Optional single-ended operation is possible by forcing a voltage on the PWC+ pin while leaving the PWC- pin unconnected. When PWC- is connected to ground, the pulse-width control circuit is automatically disabled.

Modulation Output Enable

The MAX3942 incorporates a modulation current-enable input. When MODEN is low or floating, the modulation outputs OUT+ and OUT- are enabled. When MODEN is high, the drive current is switched to OUT+. The typical enable time is 2ns and the typical disable time is 2ns.

Design Procedure

Programming the Modulation Voltage

The modulation voltage results from I_{MOD} passing through the load impedance (Z_L) in parallel with the internal 50Ω termination resistor (R_{OUT}):

$$V_{MOD} \approx I_{MOD} \times \frac{Z_L \times R_{OUT}}{Z_L + R_{OUT}}$$

To program the desired modulation current, force a voltage at the MODSET pin (see the *Typical Application Circuit*). The resulting I_{MOD} current can be calculated by the following equation:

$$I_{MOD} \approx \frac{V_{MODSET}}{11.1\Omega} + 37mA$$

An internal, independent current source drives a constant 37mA to the modulation circuitry and any voltage above V_{EE} on the MODSET pin adds to this. The input impedance of the MODSET pin is typically 20kΩ. Note that the minimum output voltage is V_{EE} + 1.9V.

Programming the Pulse-Width Control

Three methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width may be set with a 2kΩ potentiometer with the center tapped to V_{EE} (or equivalent fixed resistors), or by applying a voltage to the PWC+ pin, or by applying a differential voltage across the PWC+ and PWC- pins. See Table 1 for the desired effect of the pulse-width setting. Pulse width is defined as (positive pulse width)/((positive pulse width + negative pulse width)/2).

Input Termination Requirement

The MAX3942 data and clock inputs are CML compatible. However, it is not necessary to drive the IC with a standard CML signal. As long as the specified input voltage swings are met, the MAX3942 operates properly.

Applications Information

Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3942 output and the modulator as short as possible. Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs, as well as for the data output.

Table 1. Pulse-Width Control

PULSE WIDTH (%)	R_{PWC+}, R_{PWC-} FOR $R_{PWC+} + R_{PWC-} = 2k\Omega$	V_{PWC+} (PWC- OPEN) (V)	$V_{PWC+} - V_{PWC-}$ (V)
100	$R_{PWC+} = R_{PWC-}$	V_{EE} + 1	0
>100	$R_{PWC+} > R_{PWC-}$	> V_{EE} + 1	>0
<100	$R_{PWC+} < R_{PWC-}$	< V_{EE} + 1	<0

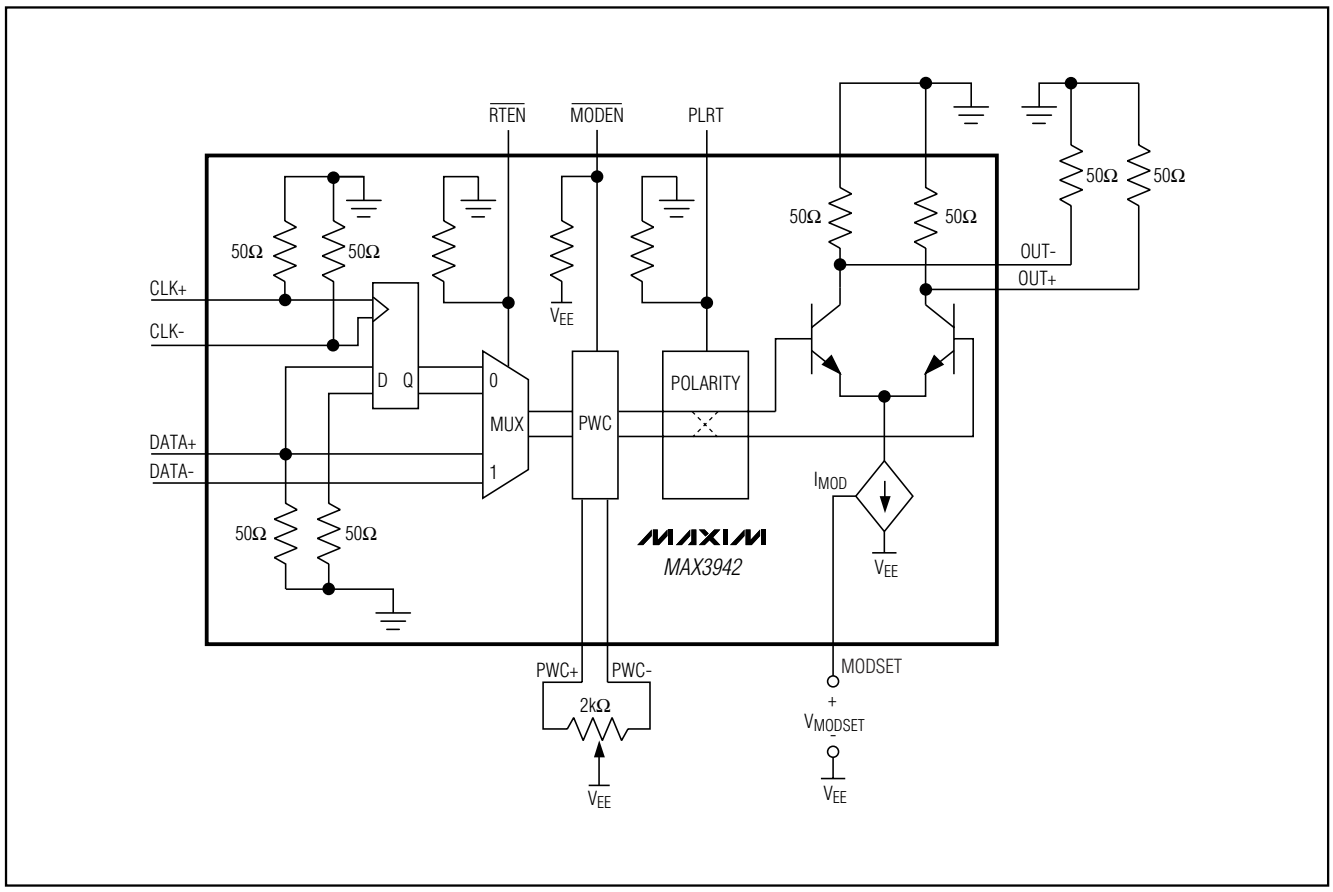


Figure 4. Functional Diagram

Interface Schematics

Figures 5 and 6 show simplified input and output circuits of the MAX3942 modulator driver.

To minimize inductance, keep the connections from OUT, GND, and V_{EE} as short as possible. This is crucial for optimal performance.

Laser Safety and IEC 825

Using the MAX3942 EAM driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each customer must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

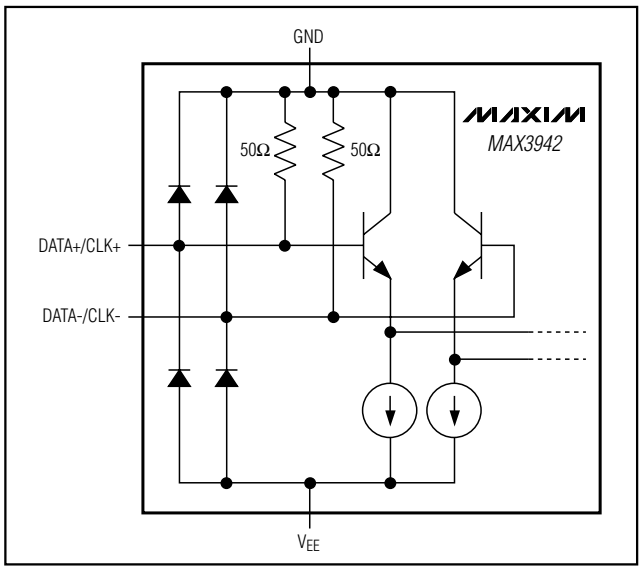


Figure 5. Simplified Input Circuit

10Gbps Modulator Driver

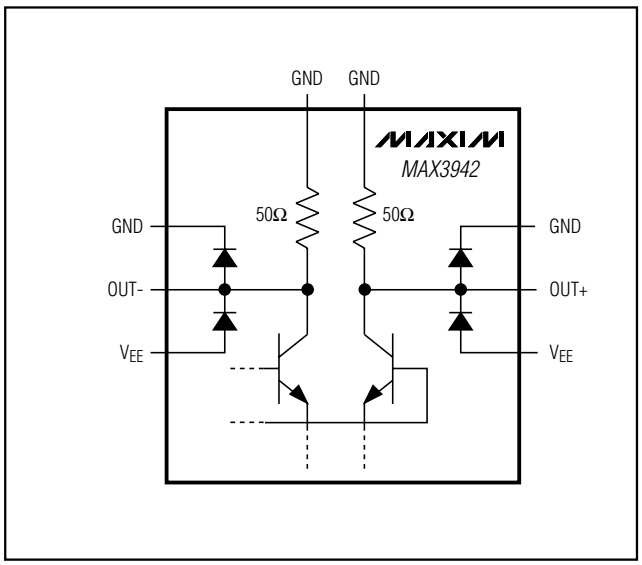
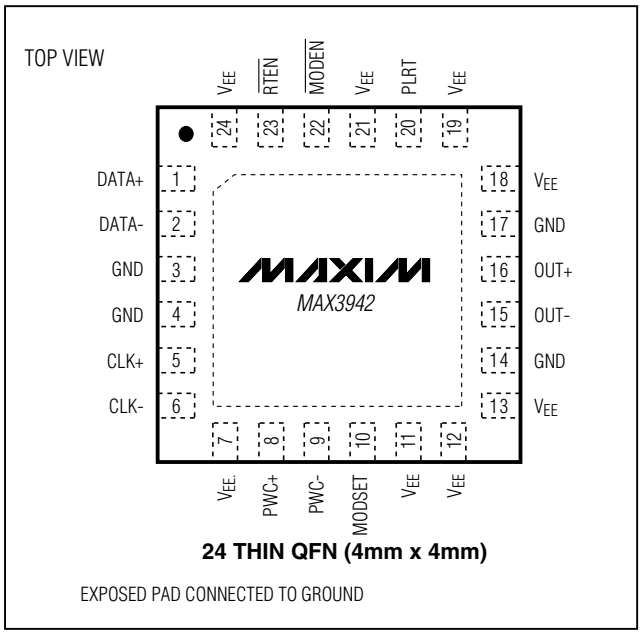


Figure 6. Simplified Output Circuit

Pin Configuration



24 THIN QFN (4mm x 4mm)

EXPOSED PAD CONNECTED TO GROUND

Exposed-Pad Package

The exposed pad on the 24-pin QFN provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3942 and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note *HFAN-08.1: Thermal Considerations for QFN and Other Exposed-Pad Packages* for additional information.

Chip Information

TRANSISTOR COUNT: 1918

PROCESS: SiGe Bipolar

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PART	PACKAGE TYPE	PACKAGE CODE
MAX3942ETG	24 Thin QFN (4mm x 4mm x 0.8mm)	T2444-1